Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2033386	divid$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:10
L2	999285	clock$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:10
L3	260783	1 and 2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:12
L4	96158	limit$4 SAME amplitude	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:12
L5	11082	3 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:13
L6	585	delay adj matching	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:13
L7	19	5 and 6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:13
L8	103796	steady adj state	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:14

L9	8	7 and 8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:17
L10	4315	clock adj buffer$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:18
L11	8338	divid$4 adj clock$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:19
L12	277	10 and 11	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:19
L13	14	12 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:19
L14	9	13 not 9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:20
L15	15729	amplitude near1 adjust$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:21
L16	7	15 and 12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:23

L17	14	12 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:24
L18	1362	limit$4 SAME amplitude SAME (steady adj state)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:25
L19	617	18 and 1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:29
L20	150	19 and 2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:28
L21	0	out adj of adj phase	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:28
L22	7786582	(out of phase)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:29
L23	276	2 and 18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/03 13:29

⊕ Sterne Kessler
Goldstein Fox
ATTORNEYS AT LAW

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To: **USPTO**

Attention: Examiner M. Ton

From: Jason D. Eisenberg

Pages (including cover sheet): 5

Fax No: (571) 273-1754

Date: March 3, 2005

Re: Appl. No. 10/622,708; Filed 07/21/03
For: **Apparatus and Method for Delay
Matching of Full and Divided Clock
Signals**
Inventor: Kwang Y. Kim

Your Reference: 10/622,708

Our Reference: 1875.1710002

Message

The European Search Report and Japanese Abstract filed on January 19, 2005 are attached.

If any portion of this transmission is not received clearly or in full,
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BP12P207EP

Anmeldung Nr./Application No./Demande n°./Patent Nr./Patent No./Brevet n°.
02256374.6-2215-

Anmelder/Applicant/Demandeur/Patentinhaber/Proprietor/Titulaire
Broadcom Corporation

COMMUNICATION

The European Patent Office herewith transmits as an enclosure the European search report for the above-mentioned European patent application.

If applicable, copies of the documents cited in the European search report are attached.

☒ Additional set(s) of copies of the documents cited in the European search report is (are) enclosed as well.

The following specifications given by the applicant have been approved by the Search Division:

☒ abstract   ☒ title

☐ The abstract was modified by the Search Division and the definitive text is attached to this communication.

The following figure will be published together with the abstract: 3

REFUND OF THE SEARCH FEE

If applicable under Article 10 Rules relating to fees, a separate communication from the Receiving Section on the refund of the search fee will be sent later.

European Patent Office

EUROPEAN SEARCH REPORT

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 175 752 A (YOKOMIZO KOICHI) 29 December 1992 (1992-12-29) * figure 3 *	1,2,4-6, 9,12,13	H03K5/13
X	PATENT ABSTRACTS OF JAPAN vol. 0131, no. 73 (E-748), 24 April 1989 (1989-04-24) & JP 64 002417 A (MITSUBISHI ELECTRIC CORP), 6 January 1989 (1989-01-06) * abstract; figure 1 *	1,4	

	TECHNICAL FIELDS SEARCHED (Int.Cl.7)
	H03K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	27 December 2004	Brown, J

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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D : document cited in the application
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EP 02 25 6374

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The members are as contained in the European Patent Office EDP file on
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27-12-2004

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 5175752	A	29-12-1992	JP	4151912 A	25-05-1992
JP 64002417	A	06-01-1989	NONE		

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER   : 64002417
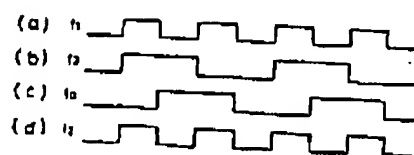PUBLICATION DATE   : 06-01-89
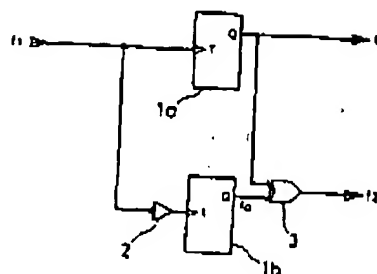
APPLICATION DATE   : 24-06-87
APPLICATION NUMBER   : 62158279

APPLICANT : MITSUBISHI ELECTRIC CORP;

INVENTOR : YAMASHITA SHINJI;

INT.CL.   : H03K 23/50

TITLE   : FREQUENCY DIVIDER

ABSTRACT : PURPOSE: To preclude the skew between a signal after frequency division and an original signal by generating 1/2-frequency-divided signals by a frequency dividing circuit at each timing which is 0 and $\pi/2$ each out of phase with the input signal, ORing the two frequency divided signals which differ in timing exclusively, and regenerating a signal similar to the frequency of the input signal.

CONSTITUTION: This frequency divider consists of 1st and 2nd frequency dividing circuits 1a and 1b which output frequency signals a half as large as the input signal, an inverter circuit 2 which outputs the inverted signal of the input signal, and a two-input exclusive OR circuit 3. The exclusive OR output signal f_2 between the output signal f_3 of the frequency dividing circuit 1a which inputs the input signal f_1 and the output signal f_a of the frequency dividing circuit 1b which inputs the output of the inverter circuit 2 for the input signal f_1 is generated to generate the signal f_2 similar to the frequency of the original input signal f_1. The signal delay propagation of the exclusive OR circuit is smaller than that of an FF circuit, so this regenerated signal f_2 is used instead of the original input signal f_1. Consequently, the skew between the original frequency signal and 1/2 frequency signal is reduced.